**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| In re Patent Application:<br>Rajeev Joshi et al.<br><br>Serial No.: 10/731,453<br><br>Filed: December 9, 2003<br><br>For: WAFER-LEVEL CHIP SCALE PACKAGE AND METHOD FOR FABRICATING AND USING THE SAME | Confirmation No. 4432<br><br>Group Art Unit: 2891<br><br>Office: Zarnecke, David A. |

Mail Stop Non-Final Response
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

**AMENDMENT AND REQUEST FOR RECONSIDERATION**

In response to the Office Action mailed January 5, 2009, Applicant requests reconsideration of this application in light of the following amendments and remarks. Filed herewith is a petition for two-month extension of time to extend the period for response to this Office Action until June 5, 2009.

**Amendments to the Claims** begin on page 2 of this paper.

**Remarks** begin on page 7 of this paper.